



Design Metrics in VLSI Design

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

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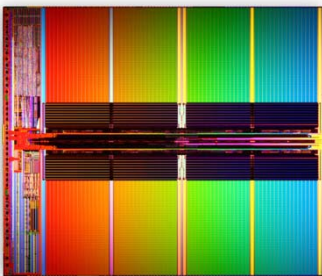
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, ...)?
 - » Cost
 - » Reliability
 - » Scalability
 - » Speed (delay, operating frequency)
 - » Power dissipation
 - » Energy to perform a function

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Design Metrics

- 34 nm 32 GbFlash memory chip (Intel)



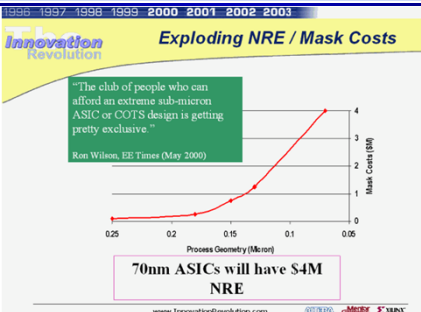
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Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
 - » design time and effort, mask generation
 - » one-time cost factor
- Recurrent costs
 - » silicon processing, packaging, test
 - » proportional to volume
 - » proportional to chip area

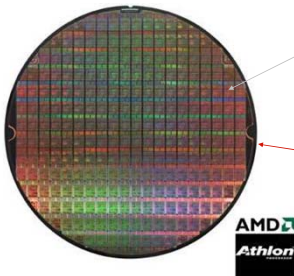
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NRE Cost is Increasing



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Die Cost

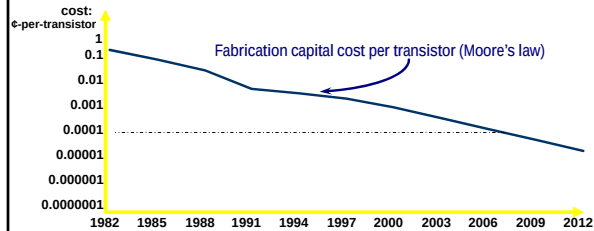


Going up to 12" (30cm)

From <http://www.amd.com>

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Cost per Transistor



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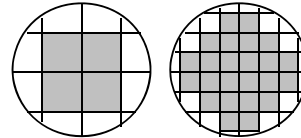


Yield

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

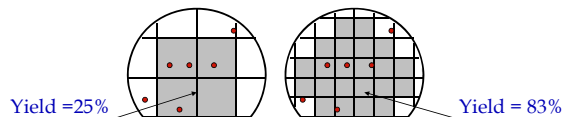
$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} = \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



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Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

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Yield Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./cm ²	Area mm ²	Dies/wafer	Yield	Die cost
386DX	2	0.90	\$900	1.0	43	360	71%	\$4
486 DX2	3	0.80	\$1200	1.0	81	181	54%	\$12
Power PC 601	4	0.80	\$1700	1.3	121	115	28%	\$53
HP PA 7100	3	0.80	\$1300	1.0	196	66	27%	\$73
DEC Alpha	3	0.70	\$1500	1.2	234	53	19%	\$149
Super Sparc	3	0.70	\$1700	1.6	256	48	13%	\$272
Pentium	3	0.80	\$1500	1.5	296	40	9%	\$417

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Example

- You want to start a company to build a wireless communications chip. How much venture capital must you raise?
- Because you are smarter than everyone else, you can get away with a small team in just two years:
 - Seven digital designers
 - Three analog designers
 - Five support personnel

From lecture : Scaling and Economics by David Harris

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Solution

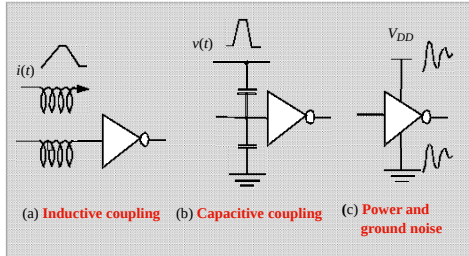
- Digital designers:
 - \$70k salary
 - \$30k overhead
 - \$10k computer
 - \$10k CAD tools
 - Total: \$120k * 7 = \$840k
- Analog designers
 - \$100k salary
 - \$30k overhead
 - \$10k computer
 - \$100k CAD tools
 - Total: \$240k * 3 = \$720k
- Support staff
 - \$45k salary
 - \$20k overhead
 - \$5k computer
 - Total: \$70k * 5 = \$350k
- Fabrication
 - Back-end tools: \$1M
 - Masks: \$1M
 - Total: \$2M / year
- Summary
 - 2 years @ \$3.91M / year
 - \$8M design & prototype

From lecture : Scaling and Economics by David Harris

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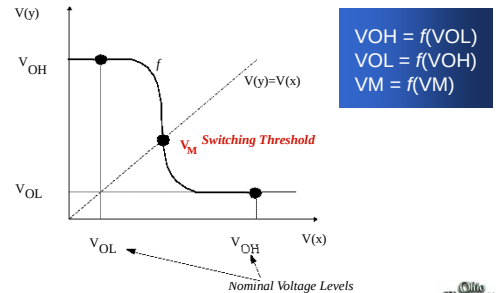
Reliability— Noise in Digital Integrated Circuits



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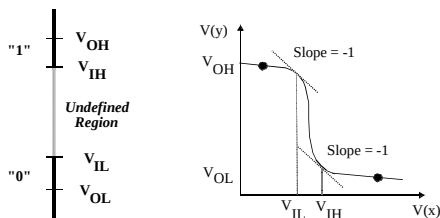
DC Operation Voltage Transfer Characteristic



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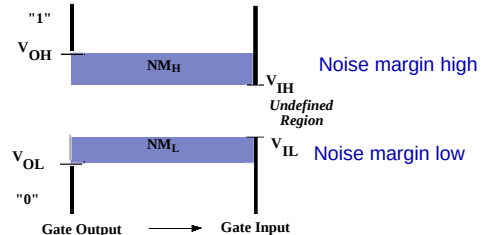
Mapping between analog and digital signals



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Definition of Noise Margins



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Noise Budget

- Allocates gross noise margin to expected sources of noise
- Differentiate between fixed and proportional noise sources
- Sources: supply noise, cross talk, interference, offset
- Shielding: metal lines and guard rings used to lower signal interference

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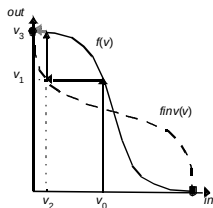
Key Reliability Properties

- Absolute noise margin values are deceptive
 - » a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

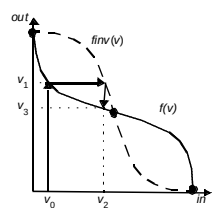
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Regenerative Property



Regenerative

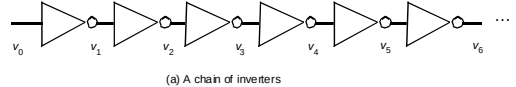


Non-Regenerative

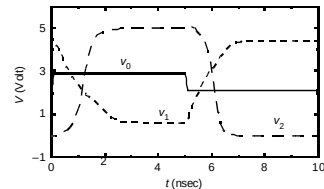
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Regenerative Property



(a) A chain of inverters



(b) Simulated response of chain of MOS inverters

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Fan-in and Fan-out

•Fan-out:

- Number of load gates, N , that are connected to the output of the driving gate
- tends to **lower** the logic levels
- deteriorates dynamic **performance**
- gate must have **low output resistance** to drive load
- library cells have **maximum fan-out** specification

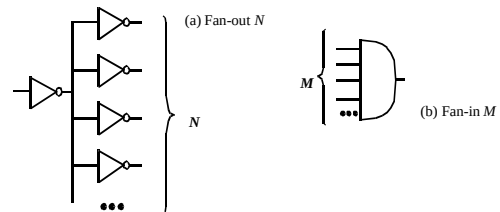
•Fan-in:

- Number of inputs, M , to the gate
- large fan-in gates are more **complex**
- results in inferior static and dynamic **performance**

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Fan-in and Fan-out



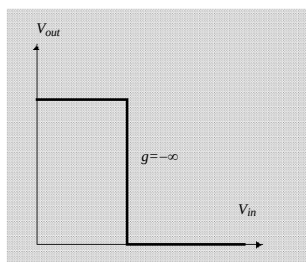
(a) Fan-out N

(b) Fan-in M

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The Ideal Gate



Characteristics

$$R_i = \infty$$

$$R_o = 0$$

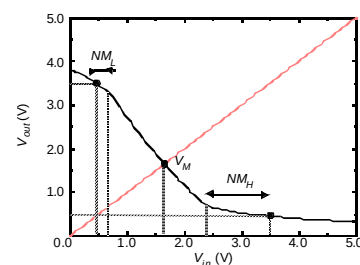
$$\text{Fanout} = \infty$$

$$NM_H = NM_L = V_{DD}/2$$

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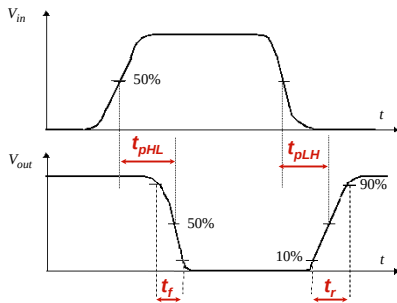
An Old-time Inverter



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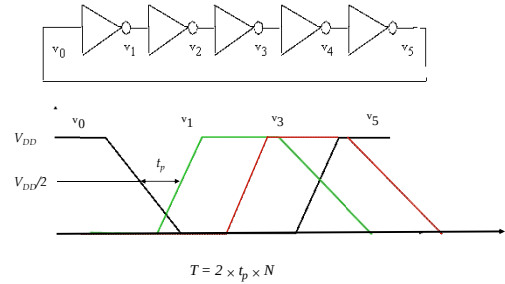


Delay Definitions



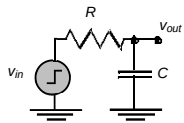
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Ring Oscillator



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A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau}) V$$

$$t_p = \ln(2) \tau = 0.69 RC$$

Important model - matches delay of inverter

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Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T} \int_t^{t+T} p(t) dt = \frac{V_{supply}}{T} \int_t^{t+T} i_{supply}(t) dt$$

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Energy and Energy-Delay

Power-Delay Product (PDP) =

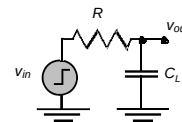
$$E = \text{Energy per operation} = P_{av} \times t_p$$

Energy-Delay Product (EDP) =

$$\text{quality metric of gate} = E \times t_p$$

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A First-Order RC Network



$$E_{0 \rightarrow 1} = \int_0^T P(t) dt = V_{dd} \int_0^T i_{supply}(t) dt = V_{dd} \int_0^T C_L dV_{out} = C_L \cdot V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t) dt = \int_0^T V_{out} i_{cap}(t) dt = \int_0^T C_L V_{out} dV_{out} = \frac{1}{2} C_L \cdot V_{dd}^2$$

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Summary

- Digital integrated circuits have come a long way and still have some potential left for the coming decades
- Some interesting challenges ahead
 - » Getting a clear perspective on the challenges and potential solutions
 - » Understanding the design metrics that govern digital design is crucial
 - » Optimize the design metrics - cost, reliability, speed, power and energy dissipation

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